# CLAIMS

1. A programmable clock generator to deliver, using a primary clock signal of determined frequency and period, a first clock signal having a frequency that is equal to the frequency of the primary clock signal divided by a set point M, the generator comprising:

means for modulating a period of the pulses of the first clock signal, wherein the set point M is a decimal number comprising a whole part M1 and a decimal part M2, so that the duration of Ni successive pulses is substantially equal to M*Ni times the period of the primary clock signal, Ni being a reference number for the modulation of the period of the pulses of the first clock signal.

2. The clock generator according to claim 1, comprising means for delivering a second clock signal the frequency of which is equal to the frequency of the first clock signal divided by a number N.

3. The clock generator according to claim 2 wherein Ni is equal to N.

4. The clock generator according to claim 1 wherein the decimal part M2 of the set point M is a binary coded rational number representing a fraction that can be modulated by increments equal to 1/Ni.

5. The clock generator according to claim 4 wherein the decimal part M2 is a fraction between -(Ni-1)/(2*Ni) and +0.5 or between –0.5 and +(Ni-1)/(2*Ni) by increments equal to 1/Ni.

6. The clock generator according to claim 4, further including a circuit receiving at its input the whole part M1 of the set point and the numerator of the rational decimal part M2 of the set point.

7. The clock generator according to claim 1, comprising means for modulating the period of the pulses of the first clock signal, arranged to deliver pulses of the first clock signal the period of which is equal to the period of the primary clock signal multiplied by a whole number the value of which is variable.

8. The clock generator according to claim 7 wherein the modulation means are arranged to deliver pulses of the first clock signal the period of which is modulated on two values equal to M1*To and (M1+1)*To, To being the period of the primary clock signal.

9. The clock generator according to claim 7 wherein the modulation means are arranged to deliver pulses of the first clock signal the period of which is modulated on two values equal to M1*To and (M1-1)*To, To being the period of the primary clock signal.

10. The clock generator according to claim 7 wherein the modulation means are arranged to deliver pulses of the first clock signal the period of which is modulated on three values (M1-1)*To, M1*To and (M1+1)*To, To being the period of the primary clock signal.

11. The clock generator according to claim 7 wherein the modulation means (comprise:

a multiplexer circuit receiving at input several division set points the value of which varies by whole increments around the whole part M1 of the set point M, delivering a set point of variable value selected from the several division set points, and

a divider of the frequency of the primary clock signal receiving at one input the variable value set point selected by the multiplexer circuit.

12. The clock generator according to claim 7 wherein the modulation means are driven by a modulation distribution circuit arranged to distribute in a determined manner, in a group of Ni successive pulses, the pulses having their period modulated.

13. The clock generator according to claim 12 wherein the distribution circuit first modulates the period of the first and last pulses out of a group of Ni successive pulses of the first clock signal, and gives the period of the middle pulses of the group of Ni pulses a non-modulated value.

14. The clock generator according to claim 12 wherein when M2 is higher than 0.5 the distribution circuit modulates the period of the pulses of the first clock signal by lower values by using the value To*(M1+1) as a non-modulated value, To being the period of the primary clock signal.

15. The clock generator according to claim 12 wherein when M2 is lower than 0.5 the distribution circuit modulates the period of the pulses of the first clock signal by higher values by using the value To*(M1) as a non-modulated value, To being the period of the primary clock signal.

16. The clock generator according to claim 12 wherein the distribution circuit comprises a hard-wired logic block receiving the decimal part M1 of the set point M at input and delivering to the modulation means, upon each new pulse of the first clock signal, a select signal for selecting the whole number determining the period of the pulse of the first clock signal.

17. A universal asynchronous receiver transceiver circuit, comprising:

a programmable clock generator to deliver, using a primary clock signal of determined frequency and period, a first clock signal having a frequency that is equal to the frequency of the primary clock signal divided by a set point M, the generator comprising means for modulating a period of the pulses of the first clock signal, wherein the set point M is a decimal number comprising a whole part M1 and a decimal part M2, so that the duration of Ni successive pulses is substantially equal to M*Ni times the period of the primary clock signal, Ni being a reference number for the modulation of the period of the pulses of the first clock signal; and

an oversampling register linked to a data receiving terminal, the register being driven by an oversampling clock signal, wherein the first clock signal delivered by the clock generator forms the oversampling clock signal.

18. A receiver transceiver circuit according to claim 17, using a bit clock signal to receive or send data, the frequency of the bit clock signal being equal to the frequency of the first clock signal divided by the reference number Ni of the clock generator circuit.

19. A method for delivering, using a primary clock signal of determined frequency and period, a first clock signal the frequency of which is equal to the frequency of the primary clock signal divided by a set point M, comprising:

generating the set point M as a decimal number having a whole part M1 and a decimal part M2; and

modulating the period of the pulses of the first clock signal so that the duration of Ni successive pulses is substantially equal to M*Ni times the period of the primary clock signal, Ni being a reference number for the modulation of the period of the pulses of the first clock signal.

20. The method according to claim 19, comprising:

producing a second clock signal the frequency of which is equal to the frequency of the first clock signal divided by a number N.

21. The method according to claim 20 wherein Ni is equal to N.

22. The method according to claim 19 wherein the decimal part M2 of the set point M is a binary coded rational number representing a fraction that can be modulated by increments equal to 1/Ni.

23. The method according to claim 22 wherein the decimal part M2 is a fraction between -(Ni-1)/(2*Ni) and +0.5 or between –0.5 and +(Ni-1)/(2*Ni) by increments equal to 1/Ni.

24. The method according to claim 22 wherein the coding of the rational number M2 only comprises:

coding of the numerator of the rational number M2, the denominator of which is a predetermined number.

25. The method according to claim 19, further including:

multiplying the period of the primary clock signal by a whole number the value of which is variable to modulate the period of the pulses of the first clock signal.

26. The method according to claim 25, further including:

modulating the period of the pulses of the first clock signal on two values equal to M1*To and (M1+1)*To, To being the period of the primary clock signal.

27. The method according to claim 25, further including:

modulating the period of the pulses of the first clock signal on two values equal to M1*To and (M1-1)*To, To being the period of the primary clock signal.

28. The method according to claim 25, further including:

modulating the period of the pulses of the first clock signal on three values (M1-1)*To, M1*To and (M1+1)*To, To being the period of the primary clock signal.

29. The method according to claim 25, further including:

modulating the period of the pulses of the first clock signal by means of a multiplexer circuit receiving at input several division set points the value of which varies by whole increments around the whole part M1 of the set point M, and delivering a set point of variable value selected from the several division set points, and by means of a divider of the frequency of the primary clock signal receiving at one input the variable value set point selected by the multiplexer circuit.

30. The method according to claim 25 wherein the modulation of the period of the pulses of the first clock signal comprises a modulation distribution including distributing in a determined manner, in a group of Ni successive pulses, the pulses having their period modulated.

31. The method according to claim 30 wherein the modulation distribution comprises the fact of first modulating the period of the first and last pulses out of a group of Ni successive pulses, by giving the period of the middle pulses of the group a non-modulated value.

32. The method according to claim 30 wherein when M2 is higher than 0.5 the period of the pulses of the first clock signal is modulated by lower values by using the value To*(M1+1) as a non-modulated value, To being the period of the primary clock signal.

33. The method according to claim 30 wherein when M2 is lower than 0.5 the period of the pulses of the first clock signal is modulated by higher values by

using the value To*(M1) as a non-modulated value, To being the period of the primary clock signal.

34. The method for oversampling, by means of an oversampling clock signal, data received at a data-receiving terminal, characterized in that the oversampling clock signal is delivered in accordance with the method according to claim 19, using a primary clock signal of determined frequency and period.

35. The method according to claim 34, comprising the production of a bit clock signal the frequency of which is equal to the frequency of the oversampling clock signal divided by a number N.

36. The method according to claim 35 wherein Ni=N.